IN THE CLAIMS

1. (Original) A method of fabricating an isolated transistor comprising:

providing a semiconductor substrate having a device structure thereon, the device structure comprising a channel structure and a control electrode structure overlying the channel structure, the channel structure being suspended over the semiconductor substrate and underlying the control electrode structure;

depositing a channel isolation layer between the channel structure and the semiconductor substrate;

forming a current electrode dielectric isolation structure laterally disposed to the channel structure; and

depositing a current electrode structure over the current electrode dielectric isolation structure.

2. (Original) The method of claim 1 wherein the providing the semiconductor substrate and device structure comprises:

providing the semiconductor substrate;

forming a first layer of a first composition;

forming a second layer of a second composition over the first layer, the second layer for providing the channel structure;

forming a dielectric layer over the second layer; and

forming at least a portion of the control electrode structure over the dielectric layer.

3. (Original) The method of claim 2 wherein the providing the semiconductor substrate and device structure further comprises:

etching the dielectric layer and the first and second layers over a plurality of current electrode regions disposed laterally from the control electrode structure; and

etching the first layer to substantially remove the first layer from under the second layer to provide a void underlying a channel region of the device structure.

4. (Original) The method of claim 2 wherein:

forming the first layer of the first composition comprises forming silicon germanium;

forming the second layer of the second composition comprises forming silicon; and

forming the dielectric layer comprises forming silicon dioxide.

5. (Original) The method of claim 1 wherein the depositing the channel isolation layer comprises using at least one technique from the group consisting of chemical vapor deposition and plasma vapor deposition.

6. (Original) The method of claim 1 wherein the channel isolation layer comprises three sublayers, and the depositing the channel isolation layer comprises:

forming a first dielectric layer substantially around the device structure, and a second dielectric layer over the semiconductor substrate and under the channel structure, the first and second dielectric layers having a first etch characteristic; and

forming a third dielectric layer substantially around the first dielectric layer and over the second dielectric layer under the channel structure, the third dielectric layer having a second etch characteristic.

7. (Original) The method of claim 6 further comprising: removing at least a portion of the third dielectric layer to expose a top surface of the semiconductor substrate.

8. (Previously Amended) The method of claim 7 wherein the removing comprises anisotropically etching the third dielectric layer to selectively and substantially remove the third dielectric layer from over the device structure.

9. (Original) The method of claim 7 further comprising: forming a recess in the semiconductor substrate.

10. (Previously Amended) The method of claim 6 wherein:

forming the first and second dielectric layers comprises forming an oxide; and

forming the third dielectric layer comprise forming a nitride.

11. (Original) The method of claim 1 wherein the forming the current electrode dielectric isolation structure comprises:

subjecting the semiconductor substrate to an oxygen containing environment; and

oxidizing a top surface of the semiconductor substrate at least at the current electrode structure to grow an oxide isolation structure over the semiconductor substrate, the current electrode dielectric isolation structure comprising the oxide isolation structure.

12. (Original) The method of claim 11 wherein the semiconductor substrate is subjected to the oxygen containing environment through at least a portion of a dielectric layer disposed over the semiconductor substrate.

13. (Original) The method of claim 1 wherein the current electrode dielectric isolation structure is formed within the semiconductor substrate.

14. (Original) The method of claim 1 wherein the depositing current electrode structures over the current electrode structures comprises growing the current electrode structures using selective epitaxy.

15. (Original) A method of fabricating a semiconductor device, the method comprising:

forming a first dielectric isolation structure within a semiconductor substrate;

forming a second dielectric isolation structure within the semiconductor substrate;

forming a third dielectric isolation structure abutting the first and second dielectric isolation structures and between the semiconductor substrate and a crystalline structure suspended over the semiconductor substrate by a supporting structure coupled to the semiconductor substrate;

depositing a first current electrode structure over the first dielectric isolation structure; and

depositing a second current electrode structure over the second dielectric isolation structure.

16. (Previously Amended) The method of claim 15 wherein: forming the first semiconductor process and forming the second dielectric isolation structure are performed simultaneously.

17. (Original) The method of claim 15 wherein the forming the third dielectric isolation structure is performed at a different time than the forming the first dielectric isolation structure and the forming the second dielectric isolation structure.

18. (Original) The method of claim 15 wherein the forming the first dielectric isolation structure and forming the second dielectric isolation structure are performed at substantially the same time.

19. (Original) The method of claim 18 wherein the depositing the first current electrode structure and depositing the second current electrode structure are performed at substantially the same time.

20. (Original) The method of claim 15 wherein the depositing the first current electrode structure and depositing the second current electrode structure are performed at substantially the same time.

21. (Currently Amended) A method of fabricating an isolated transistor comprising:

providing a substrate;

forming a channel isolation structure underlying a channel structure;

forming a current electrode isolation structure in the substrate at each one of first and second current electrode regions disposed laterally to the channel structure, the channel isolation structure and the current electrode isolation structures being formed to adjoin; and

epitaxially growing from the channel structure a current electrode over each of the current electrode isolation structures.

22. (Original) The method of claim 21 wherein the forming the current electrode isolation structures comprises oxidizing at least a portion of the substrate.

23. (Original) The method of claim 21 wherein the channel isolation structure comprises a plurality of dielectric layers, the forming the channel isolation structure comprising:

forming a first dielectric layer under the channel structure;

forming a second dielectric layer on the semiconductor substrate; and

forming a third dielectric layer between the first and second dielectric layers.

24. (Original) The method of claim 23 wherein the forming the first dielectric layer and forming the second dielectric layer on the substrate are performed at substantially the same time.